

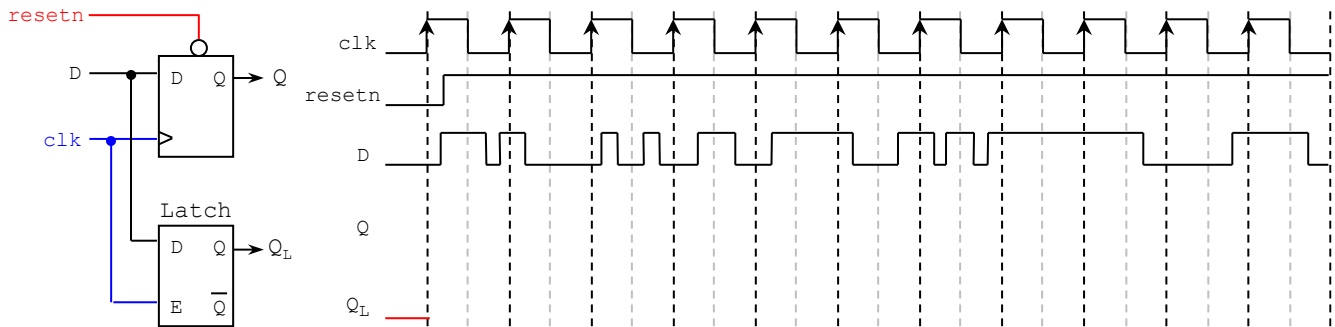
# Homework 3

(Due date: October 31<sup>st</sup> @ 11:59 pm)

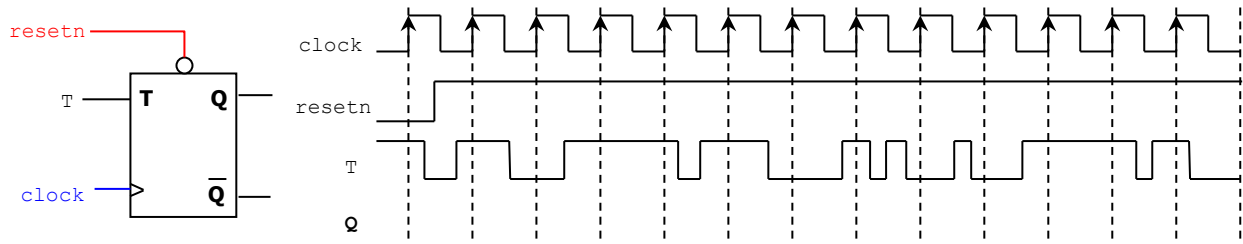
Presentation and clarity are very important! Show your procedure!

## PROBLEM 1 (11 PTS)

a) Complete the timing diagram of the circuits shown below. (5 pts)

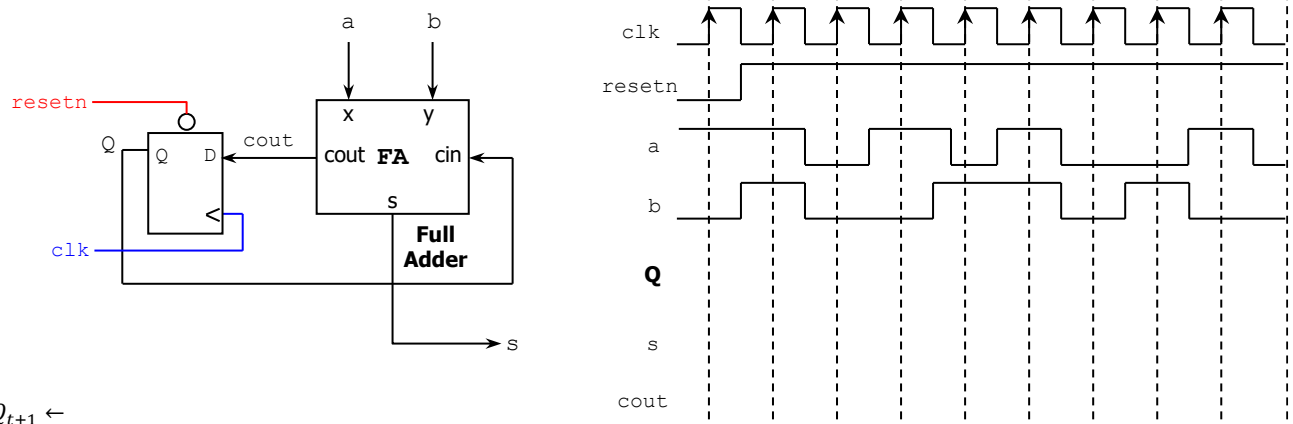


b) Complete the timing diagram of the circuit shown below: (6 pts)



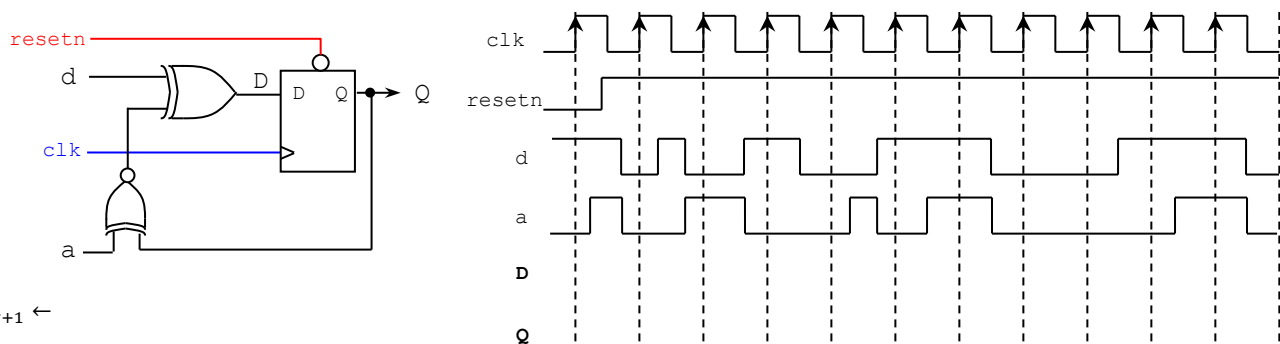
## PROBLEM 2 (17 PTS)

Complete the timing diagram of the circuit shown below. Get the excitation equation for Q (10 pts)



$Q_{t+1} \leftarrow$

Complete the timing diagram of the circuit shown below. Get the excitation equation for Q. (7 pts)



$Q_{t+1} \leftarrow$

### PROBLEM 3 (10 PTS)

- a) Complete the timing diagram of the circuit whose VHDL description is shown below. Also, get the excitation equation for  $q$ .

```
library ieee;
use ieee.std_logic_1164.all;

entity circ is
  port (prn, clk, a, x: in std_logic;
        q: out std_logic);
end circ;
```

architecture a of circ is

signal qt: std\_logic;

begin

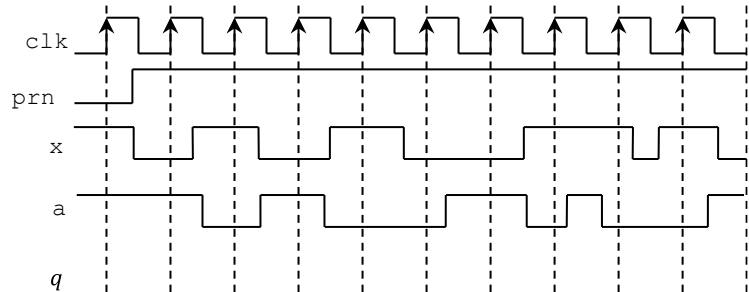
process (prn, clk, x, a)

begin

if prn = '0' then  
 qt <= '1';

```
    elsif (clk'event and clk = '1') then
      if x = '1' then
        qt <= a xnor qt;
      end if;
    end if;
  end process;
  q <= qt;
end a;
```

$q(t+1) \leftarrow$

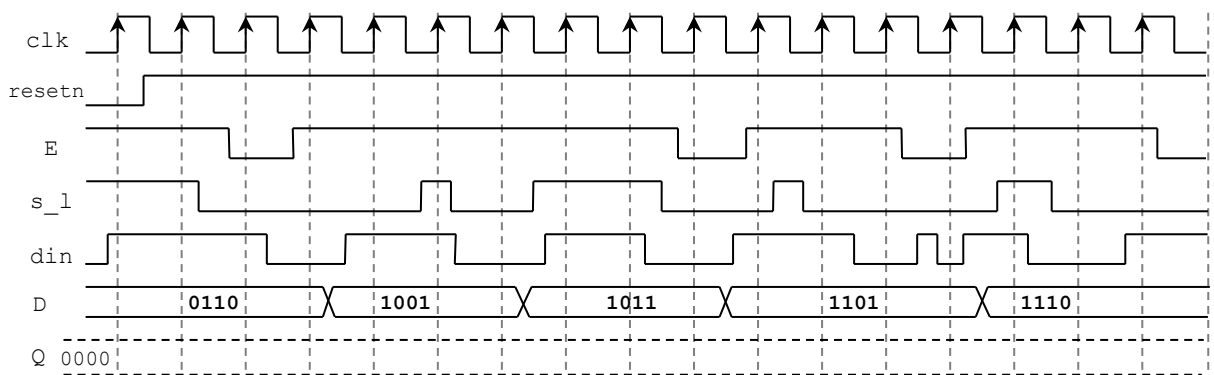
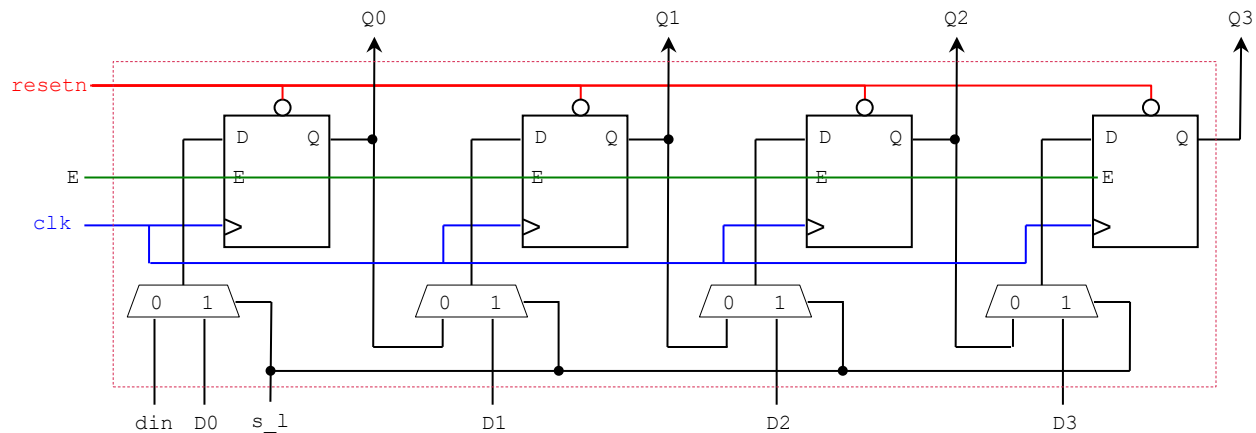


- b) With a flip flop and logic gates, sketch the circuit whose excitation equations is given by (4 pts):

$$Q(t+1) \leftarrow (x + y) \oplus Q(t)$$

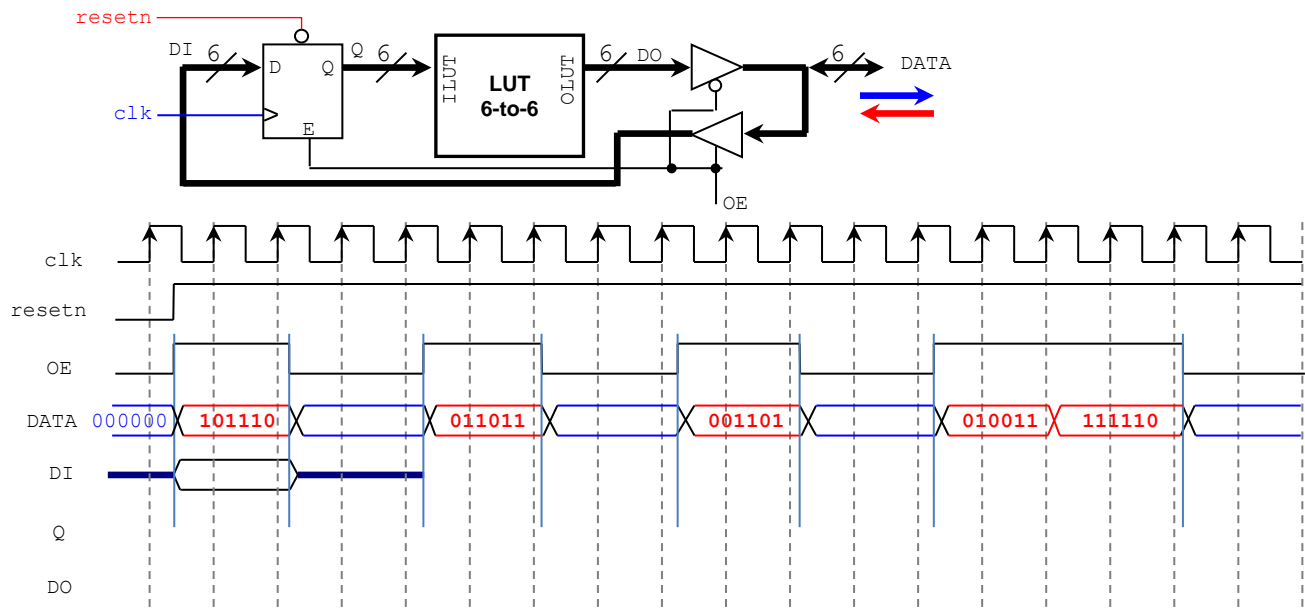
### PROBLEM 4 (10 PTS)

- Complete the timing diagram of the following 4-bit parallel access shift register with enable input.  
When  $E=1$ : If  $s_1=0$  (shifting operation). If  $s_1=1$  (parallel load) Note that  $Q = Q_3Q_2Q_1Q_0$ .  $D = D_3D_2D_1D_0$



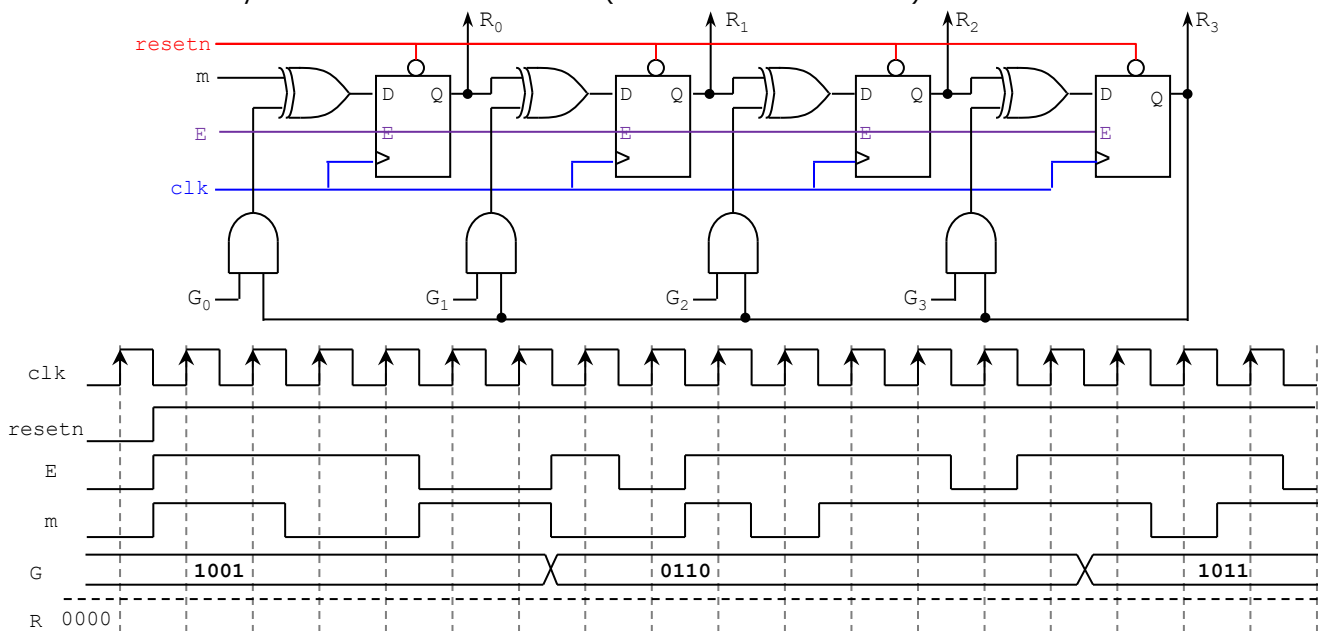
### PROBLEM 5 (12 PTS)

- Given the following circuit, complete the timing diagram (signals  $DO$ ,  $DI$ ,  $Q$ , and  $DATA$ ). The LUT 6-to-6 implements the following function:  $OLUT = [ILUT^{0.5}]$ , where  $ILUT$  is an unsigned number.  
Example:  $ILUT = 53 (110101_2) \rightarrow OLUT = [53^{0.5}] = 8 (001000_2)$



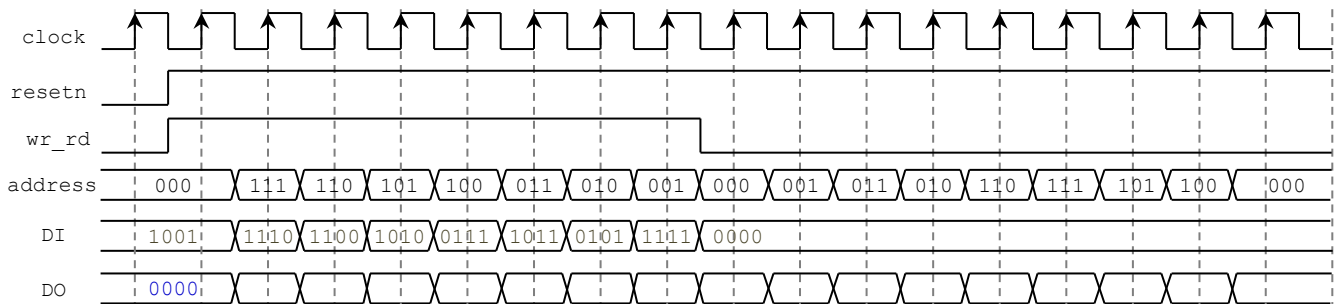
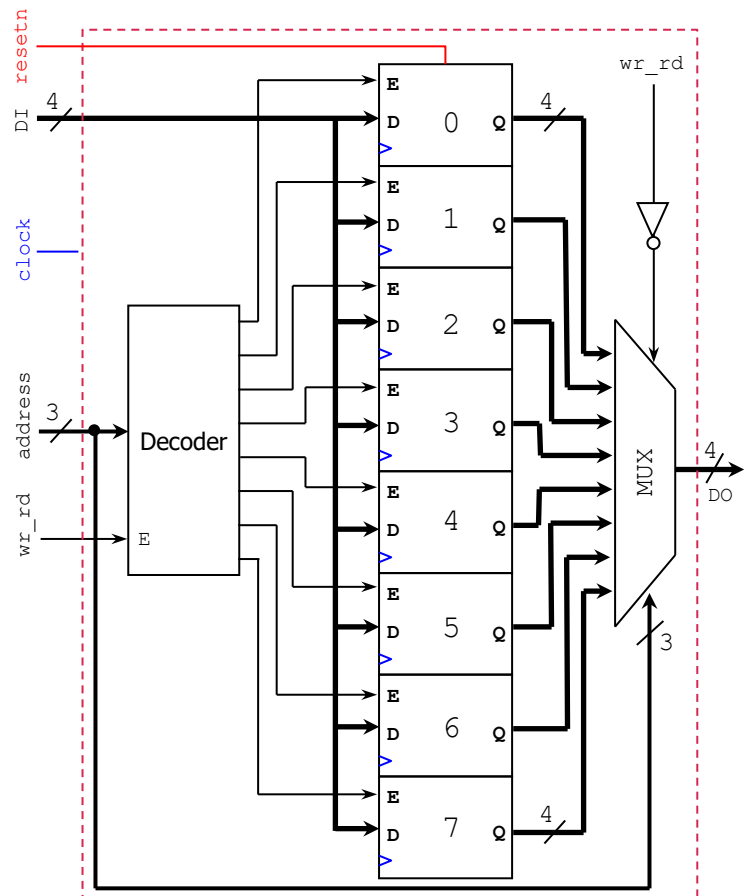
### PROBLEM 6 (22 PTS)

- For the following circuit, complete the timing diagram and get the excitation equations of the flip flop outputs.  $R = R_3R_2R_1R_0$ .  
 $R_3(t+1) \leftarrow$   
 $R_2(t+1) \leftarrow$   
 $R_1(t+1) \leftarrow$   
 $R_0(t+1) \leftarrow$
- Write the VHDL for the given circuit and simulate your circuit.
  - Write structural VHDL code. Create two files: i) flip flop, ii) top file (where you will interconnect the flip flops and the logic gates). (10 pts)
  - Write a VHDL testbench according to the timing diagram shown below (100 MHz clock with 50% duty cycle). Run the simulation (Behavioral Simulation). Verify the results: compare them with the manually completed timing diagram (8 pts)
- Upload (as a .zip file) the following files to Moodle (an assignment will be created):
  - VHDL code files and testbench.
  - A screenshot of your Vivado simulation results for (it should all the values for R).



### PROBLEM 7 (8 PTS)

- Complete the timing diagram (output DO) of the following Random Memory Access (RAM) Emulator.
- RAM Emulator: It has 8 addresses, where each address holds a 4-bit data. The memory positions are implemented by 4-bit registers. The *resetn* and *clock* signals are shared by all the registers. Data is written or read onto/from one of the registers (selected by the signal address).
- Operations:
  - Writing onto memory (*wr\_rd*=‘1’): The 4-bit input data (DI) is written into one of the 8 registers. The address signal selects which register is to be written.
    - For example: if address = “101”, then the value of DI is written into register 5.
    - Note that because the BusMUX 8-to-1 includes an enable input, if *wr\_rd*=1, then the BusMUX outputs are 0’s.
  - Reading from memory (*wr\_rd*=‘0’): The address signal selects the register from which data is read. This data appears on the BusMUX output.
    - For example: If address = “010”, then data from register 2 appears on BusMUX output.



### PROBLEM 8 (10 PTS)

- Attach your Project Status Report (no more than 1 page, single-spaced, 2 columns, only one submission per group). This report should contain the initial status of your project. For formatting, use the provided template (Final Project - Report Template.docx). The sections included in the template are the ones required in your Final Report. At this stage, you are only required to:
  - Include a (draft) project description and title.
  - Include a draft Block Diagram of your hardware architecture.
- As a guideline, the figure shows a simple Block Diagram. There are input and output signals, as well as internal components along with their interconnection.
  - At this stage, only a rough draft is required. There is no need to go into details: it is enough to show the tentative top-level components that would constitute your system as well as the tentative inputs and outputs.
- Only student is needed to attach the report (make sure to indicate all the team members).

